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EXAMINER
BRAGDON, REGINALD GLENWOOD

ART UNIT	PAPER NUMBER
2188	30

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/419,386	Applicant(s) FOX ET AL.	
	Examiner Reginald G. Bragdon	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 14-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,14-19 and 21-32* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *29* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement(s) received 28 July 2003 has been considered. Please see the attached PTO-1449(s).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 14-19, and 21-32 are rejected under 35 U.S.C. 102(e) as being anticipated by Winegarden et al. (6,467,009).

As per claim 1, Winegarden et al. teaches a configurable system on a chip including configurable system logic (CSL) 210 and a multi-master bus 225. See figure 2, column 3, lines 43-47, and claim 4 in column 39. Winegarden et al. teaches that the configuration process for the CSL is on in which the on-chip CPU writes the configuration data to the appropriate configuration memory locations ("controlling the multi-master system bus for configuration...on-chip central processing unit"). See column 29, lines 48-51. This same passage teaches "configuring a memory cell in the CSL", where the CPU stores information in the configuration memory. Winegarden et al. further teaches that the configuration memory can

be used as a general purpose RAM when it is not used as a configuration memory. See column 29, lines 57-60. It is an inherent feature of a RAM that the memory can be read and written (e.g. configured).

As per claim 21, Winegarden et al. teaches a configurable system on a chip including configurable system logic (CSL) 210 and a multi-master bus 225. See figure 2, column 3, lines 43-47, and claim 4 in column 39. Winegarden et al. teaches that the configuration process for the CSL is on in which the on-chip CPU initiates writes the configuration data to the appropriate configuration memory locations (steps of "initiating configuration" and "passing control"). See column 29, lines 48-51. This same passage teaches "configuring a memory cell in the CSL", where the CPU stores information in the configuration memory.

As per claims 14 and 24, Winegarden et al. teaches that the configuration memory is randomly addressable as part of the CSL address space. See column 29, lines 45-46.

As per claims 15 and 23, it is an inherent feature of a RAM that the memory can be read or written by devices attached to the system bus, such as the CPU 220 or DMA controller 230.

As per claims 16 and 25, Winegarden et al. teaches that the configuration memory is randomly addressable as part of the CSL address space. See column 29, lines 45-46.

As per claims 17 and 26, it is an inherent feature of a RAM that the memory can be read by devices attached to the system bus.

As per claims 18 and 27, it is an inherent feature of a RAM that the memory can be read or written by devices attached to the system bus, such as the CPU 220 or DMA controller 230.

As per claims 19 and 28, the system bus 225 is used for configuration from the CPU to the CSL as detailed in column 29, lines 48-51. The system bus 225 is also used for general interconnection as detailed at column 4, lines 32-35.

As per claim 22, Winegarden et al. teaches that the on-chip CPU is used for configuring the CSL.

As per claim 29, it is inherent that when using the configuration memory in a configuration mode or a general purpose RAM mode, the CSL must be informed, through the use of a signal, that the system bus is used to provide configuration information in a configuration mode or general data/code in a general purpose RAM mode. See column 29, lines 57-60, for a discussion of using the configuration memory as a general purpose RAM.

As per claim 30, Winegarden et al. teaches a configurable system on a chip including configurable system logic (CSL) 210 and a multi-master bus 225. See figure 2, column 3, lines 43-47, and claim 4 in column 39. Winegarden et al. teaches that the configuration process for the CSL is on in which the on-chip CPU writes the configuration data to the appropriate configuration memory locations ("initiating configuration"). See column 29, lines 48-51. This same passage teaches "configuring a memory cell in the CSL", where the CPU stores information in the configuration memory. Winegarden et al. further teaches that the configuration memory can be used as a general purpose RAM when it is not used as a configuration memory. See column 29, lines 57-60. It is an inherent feature of a RAM that the memory can be read and written (e.g. configured). It is also inherent that when using the configuration memory in a configuration mode or a general purpose RAM mode, the CSL must be informed, through the use of a signal, that the system bus is used to provide configuration

information in a configuration mode or general data/code in a general purpose RAM mode. See column 29, lines 57-60, for a discussion of using the configuration memory as a general purpose RAM.

As per claim 31, Winegarden et al. teaches that the first device and the second device are the on-chip CPU.

As per claim 32, the on-chip CPU would be the "master" of the system bus when writing information into the configuration memory.

Allowable Subject Matter

4. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

5. Applicant's arguments filed 28 July 2003 have been fully considered but they are not persuasive.

Applicant generally argues that Winegarden et al. does not teach or suggest a multi-master system bus controlled for configuration. However, Winegarden et al. teaches, as pointed out by Applicant, an on-chip CPU that writes configuration data to the appropriate configuration memory locations (column 29, lines 48-51). With reference to figure 2 of Winegarden et al., the on-chip CPU 220 is coupled to the bus 225. The bus 225 is a multi-master system bus (it is noted that figure 2 of Winegarden et al. is nearly the same as figure 2 of Applicant's

specification). The other bus masters for the bus 225 of Winegarden et al. include the DMA controller 230 and JTAG interface 240. See column 4, lines 32-34.

In Winegarden et al., the on-chip CPU 220 performs the configuration. In other words, a designer has selected the on-chip CPU 220 to perform the configuration. There is no limitation in claim 1 that prevents the "selection" from being done by a designer "statically", prior to operation of the CsoC. With respect to claim 21, as noted in the rejection of the claim, the on-chip CPU initiates the configuration and "passes" control of the multi-master bus and configuration to itself for configuring the CSL. With respect to claim 30, the on-chip CPU, part of the "group of devices" is used to configure the CSL. It is noted that "selecting" is not set forth in claim 30, merely that one of a group of devices be used to configure the CSL (where the on-chip CPU is one of those devices).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

The fax phone numbers for the organization where this application or proceeding is assigned are as follows:

(703) 746-7238 (After Final Communications)

or

(703) 746-7239 (Official Communications)

(703) 746-7240 (For Status inquiries, draft communications)

and/or

(703) 746-5693 (Use this FAX#, only after approval by the Examiner, for "INFORMAL" or "DRAFT" communications. An Examiner may request that a formal page/amendment be faxed directly to them on occasion).

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (703) 305-3823. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (703) 306-2903.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
August 8, 2003